FIG. 1

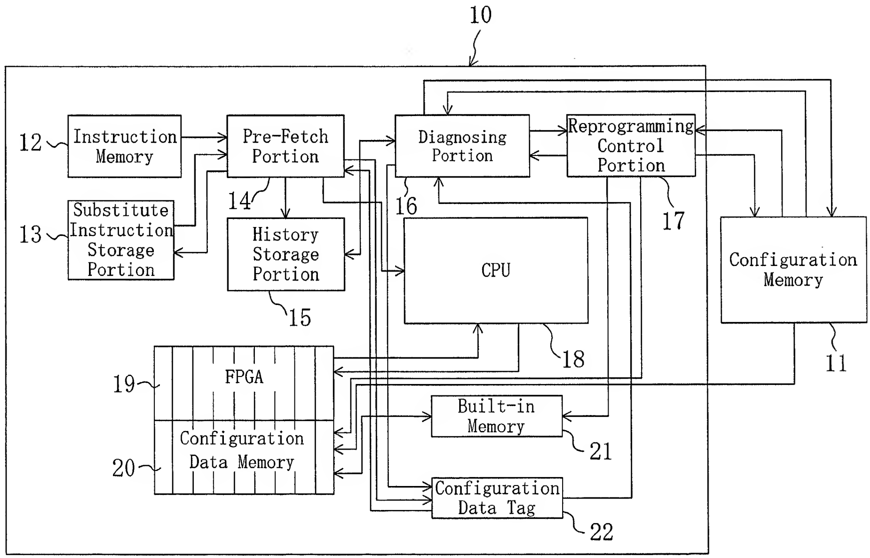

10
12
Instruction Memory
13
Substitute Instruction Storage Portion
14
Pre-Fetch Portion
15
History Storage Portion
16
Diagnosing Portion
17
Reprogramming Control Portion
CPU
18
Configuration Memory
11
19
FPGA
20
Configuration Data Memory
Built-in Memory
21
Configuration Data Tag
22

FIG. 2

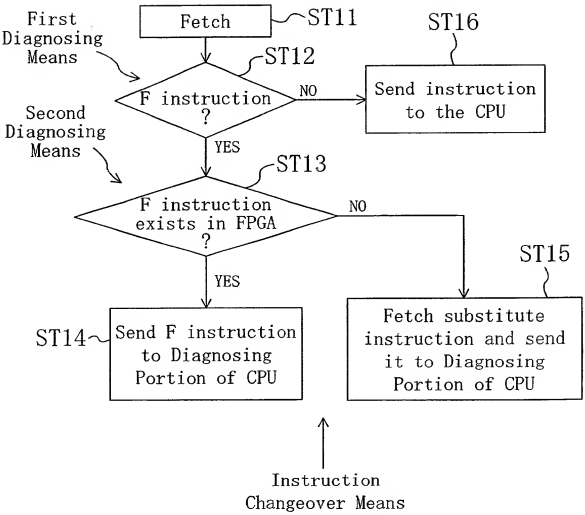

First Diagnosing Means
Fetch
ST11
ST16
ST12
F instruction ?
NO
Send instruction to the CPU
Second Diagnosing Means
YES
ST13
F instruction exists in FPGA ?
NO
ST15
YES
ST14
Send F instruction to Diagnosing Portion of CPU
Fetch substitute instruction and send it to Diagnosing Portion of CPU
Instruction Changeover Means

FIG. 3

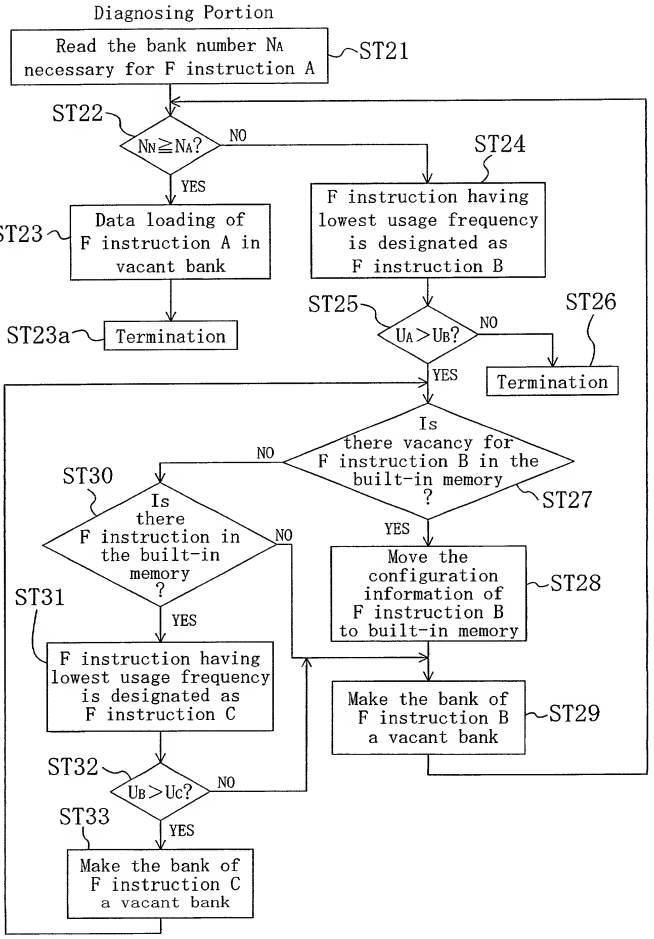

Diagnosing Portion
Read the bank number NA necessary for F instruction A
ST21
ST22
NN≧NA?
NO
YES
ST24
F instruction having lowest usage frequency is designated as F instruction B
ST23
Data loading of F instruction A in vacant bank
ST25
UA>UB?
NO
ST26
ST23a
Termination
Termination
YES
Is there vacancy for F instruction B in the built-in memory ?
NO
ST27
ST30
Is there F instruction in the built-in memory ?
NO
YES
Move the configuration information of F instruction B to built-in memory
ST28
ST31
YES
F instruction having lowest usage frequency is designated as F instruction C
Make the bank of F instruction B a vacant bank
ST29
ST32
UB>UC?
NO
ST33
YES
Make the bank of F instruction C a vacant bank

FIG. 4

Instructions		Comment
ADD	D1, D2	#D1+D2→D2
LSR	D3, D2	#D2 (D3)bit shift-right→D2

FIG. 5

Bank0 ID=1	Bank1 ID=1	Bank2 ID=4	Bank3 ID=4	Bank4 ID=4	Bank5 ID=0	Bank6 ID=0	Bank7 ID=0

FIG. 6A

```
FPGA 1 D1, D2, D3  #D1+D2 (D3)bit shift-right→D2
```

FIG. 6B

```
ADD    D1, D2      #D1+D2→D2
LSR    D3, D2      #D2 (D3)bit shift-right→D2
FPGAend            # Termination of substitute
                     instruction
```

FIG. 7

Both F instruction and substitute instruction are described.

```
FPGA 0 D1, D2, D3(addr) #D1+D2 (D3)bit shift-right→D2
                        #In case F instruction is
                         executed, skip to (addr)
ADD    D1, D2 #D1+D2→D2      Substitute instruction
                             from here
LSR    D3, D2 #D2 (D3)bit shift-right→D2 Substitute
                                         instruction up to
                                         this point
(Next instruction) # This is the address shown
                     by (addr)
```

FIG. 8

```
ADD   D1, D2     #D1+D2→D2
LSR   D3, D2     #D2 (D3)bit shift-right→D2
```

FIG. 9

ID	Instruc-tions	Corresponding Configuration Data	Number of Banks

FIG. 10

1	ADD D1, D2 LSR D3, D2	Corresponding Configuration Data	1

FIG. 11

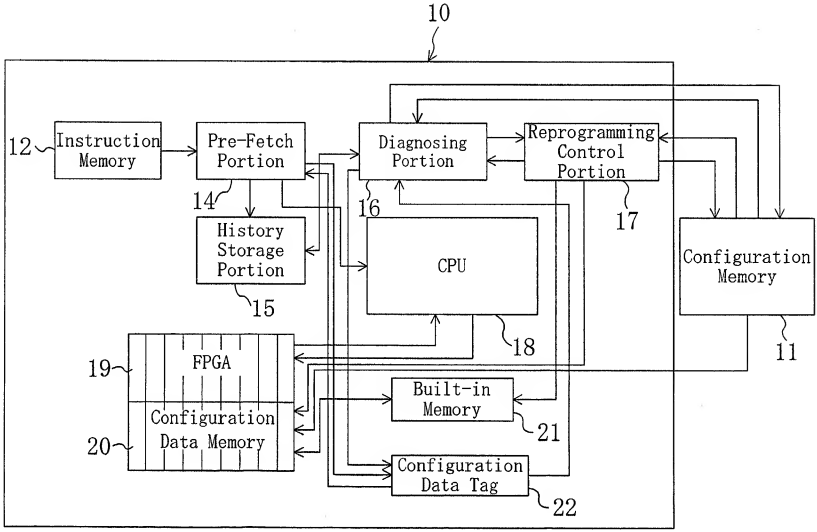

10
12
Instruction Memory
Pre-Fetch Portion
Diagnosing Portion
Reprogramming Control Portion
14
16
17
History Storage Portion
15
CPU
Configuration Memory
11
18
19
FPGA
Built-in Memory
21
Configuration Data Memory
20
Configuration Data Tag
22

FIG. 12

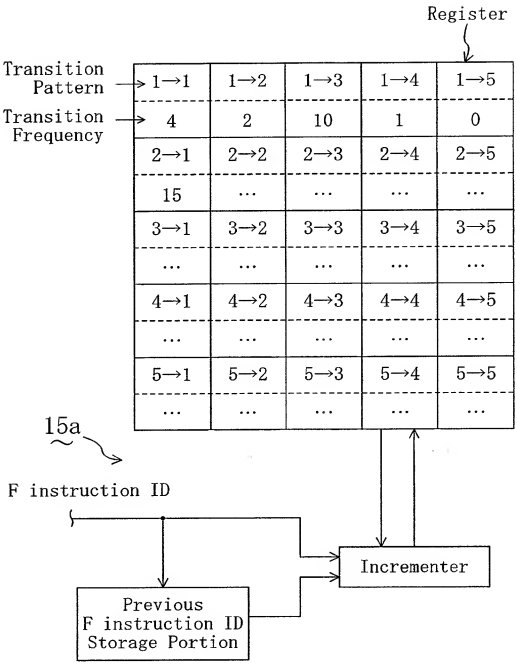
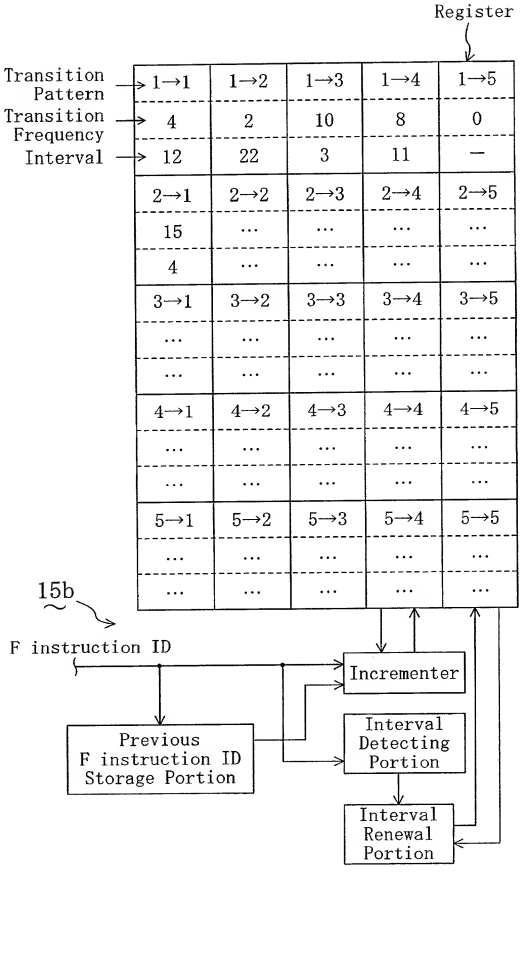

Register
Transition Pattern
Transition Frequency
1→1
1→2
1→3
1→4
1→5
4
2
10
1
0
2→1
2→2
2→3
2→4
2→5
15
3→1
3→2
3→3
3→4
3→5
4→1
4→2
4→3
4→4
4→5
5→1
5→2
5→3
5→4
5→5
15a
F instruction ID
Incrementer
Previous F instruction ID Storage Portion

FIG. 13


Register
Transition Pattern
Transition Frequency
Interval
1→1
1→2
1→3
1→4
1→5
4
2
10
8
0
12
22
3
11
—
2→1
2→2
2→3
2→4
2→5
15
4
3→1
3→2
3→3
3→4
3→5
4→1
4→2
4→3
4→4
4→5
5→1
5→2
5→3
5→4
5→5
15b
F instruction ID
Incrementer
Previous F instruction ID Storage Portion
Interval Detecting Portion
Interval Renewal Portion